CLAIMS

WHAT IS CLAIMED IS:

1. A memory system comprising:

a plurality of types of memory chips operating in synchronization with a clock signal;

a controller for outputting controller output signals to access said memory chips;

a memory controller for converting said controller output signals into memory input signals according to operation specifications of said respective memory chips, and converting memory output signals output from said memory chips into controller input signals receivable to said controller; and

a common bus for connecting said memory chips and said memory controller to transmit said memory input signals and said memory output signals.

2. The memory system according to claim 1, wherein:

said memory output signals received by said memory controller and said memory input signals received by said memory chips both through said common bus have the same input timing specification irrespective of which of said memory chips is to operate; and

said memory input signals output from said memory controller and said memory output signals output from said memory chips both through said common bus have the same output timing specification irrespective of which of said memory chips is to operate.

3. The memory system according to claim 2, wherein:

said input timing specification and said output timing specification are individually defined by a setup time and a hold time with respect to an edge of said clock signal; and

said setup time and said hold time in said output timing specification are longer than said setup time and said hold time in said input timing specification.

4. The memory system according to claim 1, wherein

said memory controller includes:

an operation memory unit for storing said operation specifications of said memory chips;

an input/output controlling unit for inputting said controller output signals fr m said controller and outputting said controller input signals to said controller, and inputting said memory output signals from said memory chips and outputting said memory input signals to said memory chips; and

a conversion control unit for operating said input/output controlling unit in accordance with information from said operation storing unit.

5. The memory system according to claim 4, wherein

said conversion control unit controls the operation timing and the input/output direction of said input/output controlling unit.

6. The memory system according to claim 4, wherein

said memory controller includes a signal holding unit for temporarily holding said controller output signals and said memory output signals received by said input/output controlling unit.

7. The memory system according to claim 6, wherein

when said memory controller receives, during operation of one of said memory chips, said controller output signal for operating another of said memory chips, said signal holding unit temporarily holds said controller output signal.

8. The memory system according to claim 6, wherein

said memory controller includes an arbiter for adjusting the order of accesses to said memory chips when access requests to said memory chips overlap.

9. The memory system according to claim 8, wherein

said arbiter is composed of programmable logics capable of reconstructing their respective circuit functions.

10. The memory system according to claim 1, wherein

said memory controller and said controller are mounted on a single chip.

11. The memory system according to claim 10, wherein

said common bus is formed on a printed-circuit board for mounting said controller and said memory chips.

12. The memory system according to claim 10, wherein:

said controller and said memory chips are stacked in three dimensions; and

said common bus is formed as interconnection wiring for connecting said controller and said memory chips.

13. The memory system according to claim 1, wherein

said memory chips include volatile memory(s) and nonvolatile memory(s).

14. The memory system according to claim 13, wherein

said volatile memory(s) is/are a clock synchronous DRAM, and said nonvolatile memory(s) is/are a clock synchronous NAND type flash memory.

15. The memory system according to claim 4, wherein

said operation memory unit is composed of programmable logics capable of rewriting information.